Subject: Re: ASIO DRIVER current status ?
Posted by mikeaudet on Tue, 25 Nov 2014 19:20:25 GMT
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Now the not so good news: Now that we can test at 64 sample buffers, there is a bug in the firmware on the EDS cards where they misreport the project time every so often.

There is code to detect this kind of thing in the PSCL. I was hoping it was a leftover from an earlier firmware or simply covering for other mistakes in the PSCL. Keep in mind, the PSCL is huge, and the whole thing is built around the assumption that the time is checked every 256 samples. This was the first time I tried to bypass the code there to check the project time directly.

This issue was easier to deal with in the PARIS app, when the sample event fired every 256 samples (an IRQ fires every 256 samples), and the buffers were 3000 samples long. If the project time reported by the EDS card looked crazy, just report 256 samples more than the last time. It will be close enough. That isn't good enough at 64 sample buffer sizes.

I'm going to have to do a bunch of profiling to see exactly how this goes wrong and for how long. Then, I can interpolate by using the windows high resolution timer.

What a mess.

Just keeping everyone in the loop.

All the best,

Mike