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Subject: Update....

Posted by [mikeaudet](#) on Thu, 19 May 2022 15:00:55 GMT

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Hi Everyone,

It's been tough to make progress this year, but I'm finally getting traction. I've just started testing a version of the PSCL that is designed to work with jBridge. For those who haven't used jBridge, it allows a 32 bit host to connect with 64 bit VST files. I just started testing it with some 64 bit Waves plugins. So far, so good. The updated PSCL has a low priority thread that checks for jBridge processes and moves them off the CPU used by the PARIS application. This way, we can run 64 bit VSTs on all but one available CPU cores, while not running into the thread-safety issues in the PARIS application.

jBridge can be found here:

<https://jstuff.wordpress.com/jbridge/>

My next move is to work on the kernel driver (scherzo.sys). I bought a new ASUS motherboard with a PCI slot, and the driver does not work with this new board. The new board uses a I/O MMU, which is a new thing for PCs. I suspect that this is the problem, but I'll know more next week. An I/O MMU puts the PCI bus behind a memory controller that has to be programmed in order to allow PCI cards to access main memory. It's an extra level of indirection put in place for security reasons. The driver was not designed for this kind of thing.

I still haven't gotten the EV security certificate. The eventually rejected by documents that were signed by a justice of the peace. It's completely insane. An accountant or a lawyer will do just fine, but a judge can't be trusted. It's nuts. I'm going to go see a notary after I get the kernel driver updated. I only get a year on the certificate, so I think it makes sense to wait until I have this next phase done.

That's all I have to report for now.

All the best,  
Mike

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## File Attachments

1) [PARIS\\_with\\_Waves.jpg](#), downloaded 3564 times

Edit  Functions  Settings  EQ  Aux  Tracks  Automation

1	2	3	4	5	6	7	8	9	10
<input checked="" type="checkbox"/> BYPASS <input checked="" type="checkbox"/> Abbey Road <input checked="" type="checkbox"/> CLA-2A Ster <input checked="" type="checkbox"/> dbx-160 Ster	<input checked="" type="checkbox"/> BYPASS <input checked="" type="checkbox"/> <<<<<<<<<<<<<<<	<input checked="" type="checkbox"/> BYPASS <input checked="" type="checkbox"/> IR-L full Ste	<input checked="" type="checkbox"/> BYPASS <input checked="" type="checkbox"/> <<<<<<<<<<<<<	<input checked="" type="checkbox"/> BYPASS <input type="checkbox"/>	<input checked="" type="checkbox"/> BYPASS <input type="checkbox"/>	<input checked="" type="checkbox"/> BYPASS <input type="checkbox"/>	<input checked="" type="checkbox"/> BYPASS <input type="checkbox"/>	<input checked="" type="checkbox"/> BYPASS <input type="checkbox"/>	<input checked="" type="checkbox"/> BYPASS <input type="checkbox"/>
EQ 1 OFF	EQ 1 OFF	EQ 1 OFF	EQ 1 OFF	EQ 1 OFF	EQ 1 OFF	EQ 1 OFF	EQ 1 OFF	EQ 1 OFF	EQ 1 OFF
Hz 1000	Hz 1000	Hz 1000	Hz 1000	Hz 1000	Hz 1000	Hz 1000	Hz 1000	Hz 1000	Hz 1000
dB 0.0	dB 0.0	dB 0.0	dB 0.0	dB 0.0	dB 0.0	dB 0.0	dB 0.0	dB 0.0	dB 0.0
BW 1.5	BW 1.5	BW 1.5	BW 1.5	BW 1.5	BW 1.5	BW 1.5	BW 1.5	BW 1.5	BW 1.5
ALL EQ	ALL EQ	ALL EQ	ALL EQ	ALL EQ	ALL EQ	ALL EQ	ALL EQ	ALL EQ	ALL EQ
EQ ON	EQ ON	EQ ON	EQ ON	EQ ON	EQ ON	EQ ON	EQ ON	EQ ON	EQ ON
OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN
L 100	R 100	L 100	R 100	L 100	R 100	L 100	R 100	L 100	R 100
SOLO MUTE	SOLO MUTE	SOLO MUTE	SOLO MUTE	SOLO MUTE	SOLO MUTE	SOLO MUTE	SOLO MUTE	SOLO MUTE	SOLO MUTE
1	2	3	4	5	6	7	8	9	10
0.0	0.0	0.0							
REC	AUTO	REC	AUTO	REC	AUTO	REC	AUTO	REC	AUTO

IR-L A: Hall - 1 (Full Reset) [A→B] Setup A Save

Full CPU

Name: Hall - 1  
 Type: Concert Hall  
 Date: 24 Mar 2004  
 SR: 96000Hz -> 44100Hz  
 Emitter: Genelec S30D

	Original	Current
Convolution:	1.85s	1.85s
RT60:	1.4s	1.4s
Channels:	4	4
Size:	11267	11267
Distance:	13m	NA

0.000Sec 2.000Sec

Reverb Time: Cnv. Start 0.000s, Cnv. Length Full  
 Latency: 11ms  
 Dry/Wet: 100  
 Direct: Off  
 Output: 0.0  
 Pre-delay: Dry, Wet

-2.8 -2.6

Options:

Maximum Files Per

Post Notifica

Transport: [Untitled Project]

P M S L 0 PUNCH LOCK

00:01:48:16.6 SMPTE  
 00:00:00:00.0 SMPTE